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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,726	01/12/2004	Chao-Hsin Lu	LUCH3011/EM	1341

23364 7590 01/28/2005

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,726	LU, CHAO-HSIN	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on line 1-5 of page 7, the recitation "the magnitude of the LVDS differential signal outputted from the differential signal output circuit 20 can be controlled through controlling the magnitude of the first control voltage V1 and the second control voltage V2 provided by the reference current control circuit 50" is misdescriptive with respect to the operation of the circuitry. It is seen that the control voltages (V1-V2, Figures 4-6) controlling the on/off of the transistors (21-24, Figures 4-6) of the output circuit so the control voltages (V1, V2) only control the phase (i.e., the timing or pulse width) of the differential signal (LVDS+, LVDS-), and are not controlling the amplitude of the differential signal. It is clearly from the operation of the circuit in Figures 4-6 that the amplitude of the differential signal (LVDS+, LVDS-) is determined based on the power supply VDD of the circuitry (i.e., the amplitude of the differential signal (LVDS+, LVDS-) is VDD). Clarification and/or appropriate correction is required.

Claim Objections

2. Claims 1-17 are objected to because of the following informalities:

Claim 1, line 3, "the phase" should be changed to --a phase-- to avoid lacking antecedent basis.

Claim 1, line 6, "the magnitude" should be changed to --a magnitude-- to avoid lacking antecedent basis.

Claims 2-17 are objected to because they include the minor informalities of claim 1.

Claim 2, line 3, "a" should be changed to --an--.

Claim 2, line 5, "the" should be deleted.

Claim 14, line 3, "a" should be changed to --an--.

Claim 14, line 5, "the" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "the magnitude of the differential signal is determined based on the control voltage" recited on the last 2 lines of the claim is indefinite because it is inconsistent with the operation of the circuit. It is seen that the control voltage (V1-V2, Figures 4-6) controlling the on/off of the transistors (21-24, Figures 4-6) of the output circuit so the control voltage (V1, V2) can only control the phase (i.e., the timing or pulse width) of the differential signal (LVDS+, LVDS-), and it is clearly from the operation of the circuit in Figures 4-6 that the amplitude of the differential signal (LVDS+, LVDS-) is determined based on the power supply VDD (i.e., the amplitude of the differential signal (LVDS+, LVDS-) is VDD). Clarification and/or appropriate correction is required.

Claims 2-7 are indefinite because they include the indefiniteness of claim 1.

Also in claim 6, "a first control voltage signal" on line 3 and "a second control voltage signal" on line 5 are indefinite because it is not clear whether they are part of the control voltage

or separate from the control voltage (recited on line 5 of claim 1). If the "first control voltage signal" and the "second control voltage signal" are separate from the control voltage, then it would requires 3 differential voltage/signal which is inconsistent with the disclosure since the disclosure only discloses two control voltages V1 and V2 (Figures 3-6). To overcome this problem, it is suggested that the recitation --of the control voltage-- be inserted after "signal" on lines 3 and 6 of claim 6.

Claims 7-12 are also indefinite because they include the indefiniteness of claim 6.

Also in claim 11, this claim is indefinite because it is not clear where the fifth to eighth transistors recited in this claim come from. Note that the previous claims only recited first to fourth transistors, and no fifth to eighth transistors. It is suggested that the fifth to eighth transistors should be deleted from claim 11.

Also in claim 12, "it" recites on line 2 is indefinite because it is not clear what "it" refers to.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-8 and 10-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lye (USP 6,566,933).

With respect to claim 1, Figure 3 of the Lye reference discloses a driving apparatus, which includes: an output circuit (70, 72) to output a differential signal (the output signals of M1-M4); a switch circuit (S5-S12) coupled to the output circuit for controlling a phase of the differential signal (controlling the on/off of M1-M4, so the phase of the differential output signal is controlled by the switched circuit); and a reference current control circuit (I2, I1, whichever circuit that provides VDD, and whichever circuit/terminal that provides reference VSS) to provide a control voltage (VDD, VSS) to the output circuit such that the magnitude of the differential signal is determined based on the control voltage.

With respect to claim 2, Figure 3 shows the output circuit (70, 72) includes a first transistor (M3), a second transistor (M4), a third transistor (M1) and a fourth transistor (M2), operational voltage source (source that provide Vdd), and ground (Vss terminal).

With respect to claim 3, Figure 3 shows the first and second transistors (M1, M2) are PMOS transistors, and the third and fourth transistors (M1, M2) are NMOS transistors.

With respect to claim 4, it is seen in the operation of Figure 3 that the control voltage (VDD, VSS) includes a first control voltage (VDD) for controlling the first and second transistors (M3, M4), and a second control voltage (VSS) for controlling the third and fourth transistors (M1, M2).

With respect to claim 5, it is seen in the operation of Figure 3 that the switch circuit (S5-S12) is for selectively turning ON either the first (M3) and fourth (M2) transistors or the second (M4) and the third (M1) transistors (i.e., when D closed switches S5, S8, S9 and S12, then D/ opened switches S6, S7, S10 and S11, so transistors M3 and M2 will be turning ON while

transistors M4 and M1 will be turning OFF; and vice versa transistors M4 and M1 will be turning ON while transistors M3 and M2 will be turning OFF).

With respect to claim 6, Figure 3 shows the switch circuit (S5-S12) includes a first switch (S5); a first control voltage signal (VSS); a second switch (S11); a second control voltage signal (VDD); a third switch (S6); a fourth switch (S12); a fifth switch (S7); a third control voltage signal (VMID); a sixth switch (S9); a fourth control voltage signal (VMID); a seventh switch (S8); and an eight switch (S10). Note that because the claim does not recited that the voltage control signals are different, therefore, for broadest reasonable interpretation, VMID can be considered as both of the claimed third and fourth control voltage signals.

With respect to claim 7, it is inherent that the apparatus in Figure 3 includes a switch control circuit (i.e., whichever circuit that is used to generated signals D and D/ for controlling the switches S5-S12) to control the operation of the first to eighth switches.

With respect to claim 8, Figure 3 shows the first and second transistors (M1, M2) are PMOS transistors, and the third and fourth transistors (M1, M2) are NMOS transistors.

With respect to claim 10, it is seen in Figure 3 that the first control voltage (VSS) and the second control voltage (VDD) are provided by the reference current control circuit (I2, I1, whichever circuit that provides VDD, and whichever circuit/terminal that provides reference VSS).

Insofar as understood in claim 11, it is seen in the operation of Figure 3 that the switch circuit (S5-S12) is for selectively turning ON either the first (M3) and fourth (M2) transistors or the second (M4) and the third (M1) transistors (i.e., when D closed switches S5, S8, S9 and S12, then D/ opened switches S6, S7, S10 and S11, so the first transistor M3 and the fourth transistor

M2 will be turning ON while the second transistor M4 and the third transistor M1 will be turning OFF; and vice versa the second and third transistors M4 and M1 will be turning ON while the first and fourth transistors M3 and M2 will be turning OFF).

With respect to claim 12, when a transistor is ON, then it operates in a triode region.

With respect to claim 13, because the driving apparatus in Figure 3 is a differential signal driving apparatus with low (minimize) power dissipation, so it meets the limitation that the driving apparatus is a LVDS driving apparatus.

With respect to claims 14-17, these claims are rejected for the same manner as discussed above with regard to claims 2-5.

Allowable Subject Matter

7. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if rewritten to overcome the rejection under 35 U.S.C. 112, 2nd paragraph, set forth above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 25, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816